Computer Architecture: High-Performance, Edge and Cloud Computing

UNIVERSITÀ
DI SIENA
1240

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LAB223 –
LABORATORIO DI ARCHITETTURA DEI CALCOLATORI

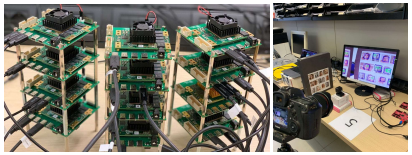
Research Activities

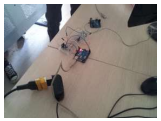
The Computer Architecture Laboratory (“Lab223” for short) focuses on the realization of the hardware/software systems that provide energy-efficient and performing solutions including:
- High-performance acceleration ranging from Multicores, GPUs, FPGAs platform
- Programming models for programmability and performance portability of parallel applications
- Energy-saving solutions based on Highly-efficient Embedded Systems
- Distributed platforms and Clusters of Heterogeneous Systems

More specifically the group has strong expertise in:

- **Architecture Modeling** (Core, Memory, Coherency & Consistency, Interconnects)
  Simulator-based, FPGA-based modeling, Educational simulators, relationship with operating-system effects
- **Accelerated Architectures**: HW-SW interface, efficiency, programmability, parallelism
- **Reconfigurable Computing**
  Dataflow-based Architectures and FPGA clusters: programmability and reliability
- **On-chip photonic networks**:
  for multi-core, memory-hierarchy, and large-scale integration needs
- **High-performance parallel programming** for CPUs, GPUs, FPGAs and accelerated architectures
- **Cybersecurity**: computer architecture and performance/efficiency viewpoint

Images





Technologies and services

- **CC-NUMA**: 64-core(x86)+1024GiB RAM, 48-core+256GiB RAM
- **HETEROGENOUS CLUSTER**: about 30 simulation servers (8-core+32GiB) @1-Gbit/s
- **FPGA-BOARDS**: 30+ Zynq-7045, Zynq Ultrascale+ (16-node cluster), PYNQ, NEXYS4, GENESYS2, ALVEO U280 (w/ HBM2)
- **ACCELERATORS**: Maxeler/Groq Dataflow computers, GPUs (TITAN, VOLTA, …)
- **EMBEDDED BOARDS**: 50+ UDOO-x86, UDOO-ARM, RASPBERRYPI, ARDUINO, …
- **RISC-V**: U740 based workstation +16GiB RAM

Applications and collaborations

CURRENTLY ACTIVE (2023+):
- cooperation with CAMPERA ELECTRONICS: development of Hardware Library (HDL) for AI applications
- participation in the BIREX++ European Digital Innovation Hub (5 universities +7 public institutions +45 enterprises):
  https://european-digital-innovation-hubs.ec.europa.eu/edih-catalogue/birex-plus-plus
- part of the HiPEAC Network of Excellence (High Performance, Edge And Cloud computing): https://www.hipeac.net/
- currently applied for the RISC-V Association Membership for open-source software and open-hardware development
- part of the CINI Embedded Systems Laboratory and High-Performance Computing Laboratory National labs
- R&D project with City University, Hong Kong for Huawei R&D, Hong Kong (about 150k€ for UNISI) on OS-architecture interaction in various contexts
- R&D project with RFI (about 110 k€ for UNISI) on EN-50128 SIL4 Software development for automatic translation of system logic into C-code
- Collaboration with GTS (ex Thales) (PhD funding) on high-performance parallel solutions for autonomous driving applications

PAST PROJECTS
HUAWEI/UNISI (UNISI=250 keuro) (2020-22) R&D project for Huawei R&D, UK
  efficient HW-SW interfacing of accelerator-based architectures and productivity
AXIOM (UNISI=1000k euro) 2015- 18 https://www.axiom-project.eu
  Modular board and software stack for Cyber-Physical Systems (with VIMAR and HERTA-SECURITIES)
TERAFLUX (UNISI=1300 keuro) 2010-14 https://teraflux.eu
  Holistic Dataflow System for the 1000 Billion transistor era (with Microsoft, Intel, HP-Labs, CAPS, Thales)
ERA: (UNISI=400k euro) 2010-13 Embedded Reconfigurable Architectures
  Reconfigurable VLIW Architecture for Smart Devices (with Evidence, ST-Microelectronics, IBM)
PHOTONICA (UNISI=140k euro) 2010-14 Integrated photonics in CMPs
  Focusing on last-level cache and cache-coherence implications
SpaceDys S.r.L.(2023): consultancy activity on the development of high-performance software for automatic space-debris identification for ESA Fly-eye telescopes

HARDWARE ARTIFACTS
● Gluon board (UNISI proprietary) carrier board to build FPGA clusters up to 255 nodes through simple USB-C 10Gbps interconnects of arbitrary topology; based on the AXIOM software stack
● RISC-V co-processor (FPGA design) for dataflow support of multi-threaded software

SOFTWARE ARTIFACTS
● COTSON2 architectural simulator enhancing HP-labs COTSON for a full-system simulation of multicore (superscalar+coherency), drive, network, devices - http://cotson.sourceforge.net
● WebRISC-V: educational software for RISC-V pipeline simulation https://webriscv.dii.unisi.it
● Phast library for productive and efficient single-source programming of multi-core CPUs and NVIDIA GPUs: https://www.phast-library.com

For more information

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